



UNITED STATES PATENT AND TRADEMARK OFFICE

clm
UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,841	11/13/2003	Rajesh Sundaram	ITL.1062US (P17921)	2553
21906 7590 05/01/2007 TROP PRUNER & HU, PC 1616 S. VOSS ROAD, SUITE 750 HOUSTON, TX 77057-2631			EXAMINER LE, THONG QUOC	
			ART UNIT 2827	PAPER NUMBER
			MAIL DATE 05/01/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/713,841

Applicant(s)

SUNDARAM ET AL.

Examiner

Thong Q. Le

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 January 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 7, 10, 11, 14-17, 19, 22-25, 27-33, 35 and 38 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10, 11, 14-17, 19, 22-25, 27-33, 35 and 38 is/are allowed.
- 6) ☒ Claim(s) 7 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Amendment filed on 01/12/2007 has been entered.
2. Claims 7,10-11,14-17,19,22-25,27-33,35-36,38 are presented for examination.

Response to Arguments

3. Applicant's arguments, with respect to 7,10-11,14-17,19,22-25,27-33,35-36,38 have been fully considered and are persuasive. The rejection of last Office action has been withdrawn.
4. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.
5. Applicant's arguments with respect to claims 7,10-11,14-17,19,22-25,27-33,35-36,38 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by Taniguchi et al. (Pub. U.S. Patent No. 2002/0074569).

Regarding claim 7, Taniguchi et al. disclose a method ([0014]) comprising:

supplying a negative voltage to at least one deselected wordline of a non-volatile memory array from a decoder coupled to the at least one deselected wordline during a

programming operation on a selected wordline (ABSTRACT, *a voltage is applied to one word line, which is set so as to serve as a selected word line, and then carries are stored in a floating gate of each selected memory cell, a negative voltage is applied to other non-selected word lines other than selected word line*, [0014], [0023] ;

providing the negative voltage and a control negative voltage to the decoder (Figure 1, XD, control CC comprises command decoder, [0060-0061]), further comprising providing the control negative voltage to a substrate of a transistor of the decoder coupled to pass the negative voltage to the at least one deselected wordline ([0013], [0016]); and

supplying a positive voltage ([0023]) to the selected wordline of the non-volatile memory array to program the selected wordline while supplying the negative voltage ([0066-0068]).

8. Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by Kataoka et al. (U.S. Patent No. 6,172,917).

Regarding claim 7, Kataoka et al. disclose method (Column 3, lines 55-65) comprising:

supplying a negative voltage to at least one deselected wordline of a non-volatile memory array from a decoder coupled to the at least one deselected wordline during a programming operation on a selected wordline (Column 3, lines 60-65, means for applying a negative voltage to word lines of memory cells which are not selected);

providing the negative voltage (Figure 11, 302) and a control negative voltage (Figure 11, 301) to the decoder (Figure 11, 306), further comprising providing the

Art Unit: 2827

control negative voltage to a substrate of a transistor of the decoder coupled to pass the negative voltage to the at least one deselected wordline (Figure 11); and

supplying a positive voltage to the selected wordline of the non-volatile memory array to program the selected wordline while supplying the negative voltage (Column 11, lines 60-64, Column 14, lines 7-31).

Allowable Subject Matter

9. Claims 10-11,14-17,19,22-25,27-33,35-36,38 are allowed.

10. Claims 10-11,14-17,19,22-25,27-33,35-36,38 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Taniguchi et al. (Pub. U.S. Patent No. 2002/0074569), Kataoka et al. (U.S. Patent No. 6,172,917) and others, does not teach the claimed invention having a decoder to supply a negative voltage to a deselected address line of a memory array, the decoder comprising a first transistor of a first polarity coupled to receive a negative control voltage and the negative voltage and to pass the negative voltage to the deselected address line, and a second transistor of a second polarity coupled to the first transistor and the deselected address line to pass a program pulse to the deselected address line if it becomes a selected address line, the decoder further comprising a pre-driver circuit to control an intermediate node coupled to a gate terminal of the first transistor and a gate terminal of the second transistor.

Art Unit: 2827

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Thong Q. Le
Primary Examiner
Art Unit 2827